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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/675,751 | 09/30/2003 | Jimmie Earl DeWitt JR. | AUS920030482US1 | 8000 |

35525 7590 01/30/2006

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| EXAMINER | |
|---|---|
| CODY, DILLON J | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | |

DATE MAILED: 01/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/675,751 | DEWITT ET AL. | |
| | Examiner | Art Unit | |
| | Dillon Cody | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/30/03, 7/1/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-25 are pending.

### *Papers Filed*

2. Examiner acknowledges receipt of claims, disclosure, drawings, declaration, and information disclosure statement, all filed 30 Sept. 2003, and a second information disclosure statement filed 1 July 2005.

### *Title*

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

### *Specification*

4. Applicant is requested to fill in the blank spaces on pages 1-2 of the specification with the now-assigned application serial numbers.

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### *Claim Objections*

6. Claims 9, 17 and 23 are objected to because of the following informalities:

Claim 9, line 1 and Claim 17, line 2: "actions" should read "action"

Claim 23, line 1: "medium" should follow "computer readable"

Appropriate correction is required.

### *Claim Rejections - 35 USC § 101*

7. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 19-25 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Pages 64-65 of the specification define "computer readable media" to include "transmission-type media". Transmission media are not tangible, and hence, non-statutory.

### *Claim Rejections - 35 USC § 102*

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

9. Claims 1-25 are rejected under 35 U.S.C. 102(a) as being anticipated by Davidson et al. (U.S. Patent No. 6,574,727) hereinafter referred to as Davidson.

10. As per claim 1, Davidson discloses a method in a data processing system for monitoring processing of instructions, the method comprising:

receiving an instruction at a processor for execution; (Col. 8 lines 58-60)

responsive to being in an enabled state, (Col. 11 lines 35-55) determining whether the instruction is associated with an indicator in a shadow memory; (Col. 8 line 65 – col. 9 line 8) *The examiner asserts that the value to be matched must be stored in some sort of memory, as the value could not be retained if it wasn't.*

and performing a selected action in response to the indicator being associated with the instruction. (Col. 8 lines 30-36)

11. As per claim 2, Davidson discloses the method of claim 1, wherein the instruction is received in an instruction cache (Fig. 4 instruction cache 406) and further comprising: executing the instruction after receiving the instruction for execution. *Examiner asserts that the instruction is executed, as indicated by the arrow entering execution unit 480 in fig. 4.*

12. As per claim 3, Davidson discloses the method of claim 1, wherein the determining step comprises: examining a register in the processor; and determining whether the register is set to indicate the enabled state. (Col. 11 lines 37-55)

13. As per claim 4, Davidson discloses the method of claim 1, wherein the selected action includes at least one of

sending the instruction to a performance monitor unit (Col. 8 lines 30-36),

sending the instruction to a data cache, *The examiner asserts that all instructions are sent to instruction cache 256 (Fig. 2) and that all instructions constitute data.*

and sending the instruction to an interrupt unit.

14. As per claim 5, Davidson discloses the method of claim 1, wherein the instruction is received in a bundle. (Col. 9 lines 22-25)

15. As per claim 6, Davidson discloses the method of claim 1, wherein the enabled state is enabled by setting a register in a processor. (Col. 11 lines 35-55)

16. As per claim 7, Davidson discloses the method of claim 1, wherein the shadow memory contains debugging information. (Col. 7 line 59-61)

17. As per claim 8, Davidson discloses a method in a data processing system for monitoring access to data during execution of instructions by a processor, the method comprising:

responsive to being in an enabled state when a data access to a memory location occurs, determining whether the memory location is associated with an indicator in a shadow memory; (Col. 4 lines 18-20) *The examiner asserts that if the*

*"sample" bit is set, the performance monitor will determine if the read/write operation references a memory location in question, stored in a MMCR.*

and performing a selected action in response to the indicator being associated with the memory location. (Col. 4 lines 30-35)

18. As per claim 9, Davidson discloses the method of claim 8, wherein the selected action is at least one of forcing an interrupt and counting accesses to the memory location. (Col. 4 lines 30-35 and Col. 5 lines 8-16) *The examiner asserts that the PMC1 is configurable to count memory accesses.*

19. As per claim 10, Davidson discloses the method of claim 8, wherein the shadow memory includes a shadow word for each word of data. *The examiner asserts that in any memory, a word of data requires at least a word of memory space to store said data. Storing a word of data in a memory location with fewer than a word of memory will cause portions of the data to be lost, causing undesired operation.*

20. As per claim 11, Davidson discloses the method of claim 8, wherein the determining step comprises: examining a register in the processor (Fig. 6 sample bit 648); and determining whether the register is set to indicate the enable state. *The examiner asserts that if the sample bit is not set, the instruction associated with it is ignored by the performance monitor.*

21. As per claim 12, Davidson discloses a data processing system for monitoring processing of instructions, the data processing system comprising: receiving means for receiving an instruction at a processor for execution (Col. 8 lines 58-60); determining means, responsive to being in an enabled state, for determining whether the instruction is associated with an indicator in a shadow memory (Col. 8 line 65 – col. 9 line 8) *The examiner asserts that the value to be matched must be stored in some sort of memory, as the value could not be retained if it wasn't*; and performing means for performing a selected action in response to the indicator being associated with the instruction. (Col. 8 lines 30-36)

22. As per claim 13, Davidson discloses the data processing system of claim 12, wherein the determining means is a first determining means and further comprises: examining means for examining a register in the processor; and second determining means for determining whether the register is set to indicate the enabled state. (Col. 11 lines 37-55)

23. As per claim 14, Davidson discloses the data processing system of claim 12, wherein the selected action includes at least one of

sending the instruction to a performance monitor unit (Col. 8 lines 30-36),

sending the instruction to a data cache, *The examiner asserts that all instructions are sent to instruction cache 256 (Fig. 2) and that all instructions constitute data.*

and sending the instruction to an interrupt unit.

24. As per claim 15, Davidson discloses the data processing system of claim 12, wherein the instruction is received in a bundle. (Col. 9 lines 22-25)

25. As per claim 16, Davidson discloses a data processing system for monitoring access to data during execution of instructions by a processor, the data processing system comprising: determining means, responsive to being in an enabled state when a data access to a memory location occurs, for determining whether the memory location is associated with an indicator in a shadow memory (Col. 4 lines 18-20) *The examiner asserts that if the "sample" bit is set, the performance monitor will determine if the read/write operation references a memory location in question, stored in a MMCR.*; and performing means for performing a selected action in response to the indicator being associated with the memory location. (Col. 4 lines 30-35)

26. As per claim 17, Davidson discloses the data processing system of claim 16, wherein the selected action is at least one of forcing an interrupt and counting accesses to the memory location. (Col. 4 lines 30-35 and Col. 5 lines 8-16) *The examiner asserts that the PMC1 is configurable to count memory accesses.*

27. As per claim 18, Davidson discloses the data processing system of claim 16, wherein the shadow memory includes a shadow word for each word of data. *The*

*examiner asserts that in any memory, a word of data requires at least a word of memory space to store said data. Storing a word of data in a memory location with fewer than a word of memory will cause portions of the data to be lost, causing undesired operation.*

28. A computer program product in a computer readable medium for monitoring processing of instructions, the computer program product comprising: first instructions for receiving an instruction at a processor for execution (Col. 8 lines 58-60); second instructions, responsive to being in an enabled state, for determining whether the instruction is associated with an indicator in a shadow memory (Col. 8 line 65 – col. 9 line 8) *The examiner asserts that the value to be matched must be stored in some sort of memory, as the value could not be retained if it wasn't*; and third instructions for performing a selected action in response to the indicator being associated with the instruction. (Col. 8 lines 30-36)

29. As per claim 20, Davidson discloses the computer program product of claim 19, wherein the second instruction comprises: first sub-instructions for examining a register in the processor; and second sub-instructions for determining whether the register is set to indicate the enabled state. (Col. 11 lines 37-55)

30. As per claim 21, Davidson discloses the computer program product of claim 19, wherein the selected action includes at least one of

sending the instruction to a performance monitor unit (Col. 8 lines 30-36),

sending the instruction to a data cache, *The examiner asserts that all instructions are sent to instruction cache 256 (Fig. 2) and that all instructions constitute data.*

and sending the instruction to an interrupt unit.

31. As per claim 22, Davidson discloses the computer program product of claim 19, wherein the instruction is received in a bundle. (Col. 9 lines 22-25)

32. As per claim 23, Davidson discloses a computer program product in a computer readable [medium] for monitoring access to data during execution of instructions by a processor, the computer program product comprising: first instructions, responsive to being in an enabled state when a data access to a memory location occurs, for determining whether the memory location is associated with an indicator in a shadow memory (Col. 4 lines 18-20) *The examiner asserts that if the "sample" bit is set, the performance monitor will determine if the read/write operation references a memory location in question, stored in a MMCR.*; and second instructions for performing a selected action in response to the indicator being associated with the memory location. (Col. 4 lines 30-35)

33. As per claim 24, Davidson discloses the computer program product of claim 23, wherein the selected actions is at least one of forcing an interrupt and counting

accesses to the memory location. (Col. 4 lines 30-35 and Col. 5 lines 8-16) *The examiner asserts that the PMC1 is configurable to count memory accesses.*

34. As per claim 25, Davidson discloses the computer program product of claim 23, wherein the shadow memory includes a shadow word for each word of data. *The examiner asserts that in any memory, a word of data requires at least a word of memory space to store said data. Storing a word of data in a memory location with fewer than a word of memory will cause portions of the data to be lost, causing undesired operation.*

***Conclusion***

35. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dillon Cody whose telephone number is 571-272-8401. The examiner can normally be reached on Mon - Fri, 8 AM - 5 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJC

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